RADIATION DETECTION ELECTRONIC SYSTEM WITH FLASH ANALOG TO DIGITAL CONVERTER (FADC) AND FIELD PROGRAMMABLE GATE ARRAY (FPGA)

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Abstract: Using an electronic device including FADC and FPGA, in this work, signals from radiation detector were processed. Such device is a combination of two electronic boards: the FADC board, which was used to convert analog signal into digital signal, and an interface board which includes the Altera FPGA. The later board was configured in order to process the trigger and transmit data to computer. With this system, each pulse (event) can be recorded and analyzed so that parameters such as pulse's area, peak of the pulse, time, etc. With obtained results, the system built in this work can be reliably applied in many radiation detection systems.

Keywords*: Flash ADC, FPGA, radiation detector*

I. INTRODUCTION:

The development of Electronic Techniques gives many advantages to the radiation detection and measurement not only the speed of acquisition but also in the way signal was processed. In this work, with new technologies as FPGA, FADC and the help of computer, those advantages can be reached. A group of Osaka University has developed a 8bits-250MHz FADC board combined with Logic Trigger interface board with the help of FPGA. As the collaboration program[1] between Graduate school of Science, Osaka University and Faculty of Physics, University of Science-HCMC, we use these equipment for the development of DAQ in the radiation detection study. Using FADC built-in board, the signals from detector were converted into 8-bits binary digits. They were, then, input the board which includes Altera FPGA chip[2] for processing and transmitting to computer. The communication between computer and electronic device via RS-232 was handled by a program written using LabVIEW software[3]. Baud rate of RS-232 in this research is 115200 bps which is not really fast. However, one important thing is that the pulse's shape can be obtained using this device, different from other traditional devices where usually only the peak of pulse was processed. So, analyzing data, we can get the area, peak, time and other useful information. In this work, the comparison between the pulse shape obtained from our device and from Agilent DSO3000 oscilloscope[4] showed a good agreement. With such result, the system developed in this work has many applications in radiation detection and measurement. Moreover, with the reconfigurable FPGA, other function can be added when further developing.

II. DEVICE CONFIGURATION:

The kit[1] includes two components: FADC board and Interface board.

The first one has four FADC chip built-in and one Xilinx FPGA chip. It converts analog signals into 8-bits binary digits which are then rearranged and transmitted to the Interface board. The clock of conversion is 250MHz, i.e. the signal is divided into many 4ns bins as illustrated in figure 1. The board has two analog inputs with 50Ω impedance according to the NIM standard. So, it can handle two signal channels and sent out four data (32bits) with clock 125MHz. The arrangement of data from two channels, which were processed by Xilinx chip, can be seen in figure 2.

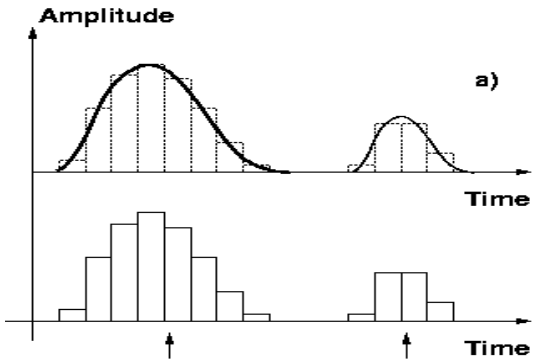


Figure 1: The conversion of FADC

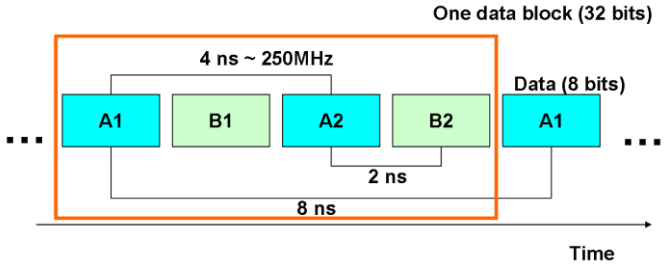


Figure 2: data arrangement of one block

The second board receives data from FADC board for triggering, rearranging and transmitting to computer. The key-component of this board is Altera FPGA chip which has to be configured to do such processes. The code for configuration was written using VHSIC hardware description language (VHDL). Quartus II software[2] was used for compiling and installing the code into FPGA via joint test action group (JTAG) port. There are also one RS-232 port for communication with computer and two fire-wire ports for further development.

III. DATA ACQUISITION:

Whole acquisition process includes hardware process and software process. Hardware process was divided into four small processes handled by four components: trigger, delay, execute, bus controller. Software to receive and store data was written with LabVIEW software. The user interface of program is shown on figure 3. Let's consider hardware processes:

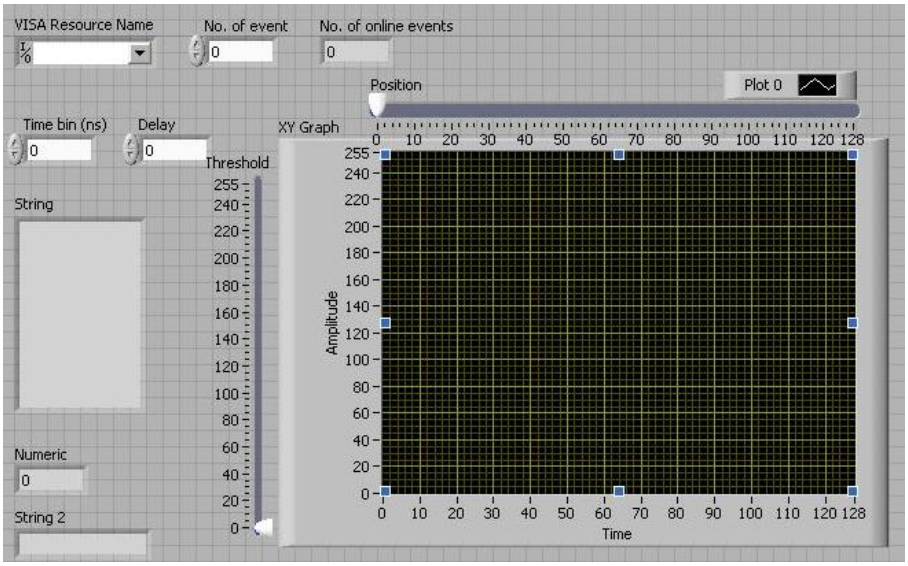


Figure 3: User interface of data acquisition program in LabVIEW software

1. Trigger:

Data was transmitted continuously from the FADC board with clock of 125MHz. However, not all of those data are important, yet only that of signal should be considered. So, ones have to set a level in order to allow only signal's data to get through. To do this, the trigger component was set up with two inputs, one for data and the other for level which received from the user. They will be compared each other. Then, one logic signal would be sent out if the peak of pulse was higher than the level. Execute and bus control components were only activated when received this logic signal.

2. Delay:

This component has only function: to delay data before being rearranged by execute component. It makes data flow slower than the real signal. The reason is that when the trigger activated bus controller and executer components, some data which go before that process were not recorded. So, in order to get the full pulse shape, ones have to delay the data flow.

3. Execute:

Default sample rate of ADC is 250MHz, i.e, input pulse was converted into one 8-bits digit each 4ns. However, if the pulse time was long, for example about 10μs(2500 times larger than 4ns), it would consume memory a lot for processing and storing data. In addition, it would take a long time to transmit them to computer, especially with RS-232. So, it necessary to reduce the data amount for each pulse to the fix size. In this work, we use 128 32-bits words for storing one pulse. That means we have to bypass some data. This can be done by repeatedly collecting one data after some clock (set by user). And that is what this component does: renormalize the data.

4. Bus controller:

Data was sent to computer using RS-232. So, a component to control this process is required. It was set up to receive instructions from computer, convert them into binary digit and then store them in registers. Reading these registers, other components can know what and how they should do. Another important function of this component is to reformat the data to follow the RS-232 standard.

IV. EXPERIMENT SET UP:

1. Test the trigger:

The purpose of this experiment is to make sure that the trigger process is accurate. To do this, pulses from High Purity Germanium (HPGe)[5] detector were amplified and then connected to the input of FADC as illustrated in figure 4. The data was then plotted to show the pulse shape. The result was shown in figure 5.

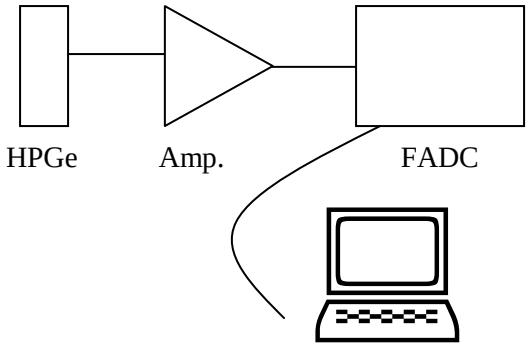


Figure 4: Trigger test experiment set up

2. Control the device:

In this step, the HPGe detector was replaced by a Pulse generator which generates negative logic pulse. Amplifier with available shaping function was used to change the time of output pulse. However, pulse time can also be changed by pulse generator. The reason to change pulse time is to make pulse with various characteristics so that the setting of user can affect in all cases.

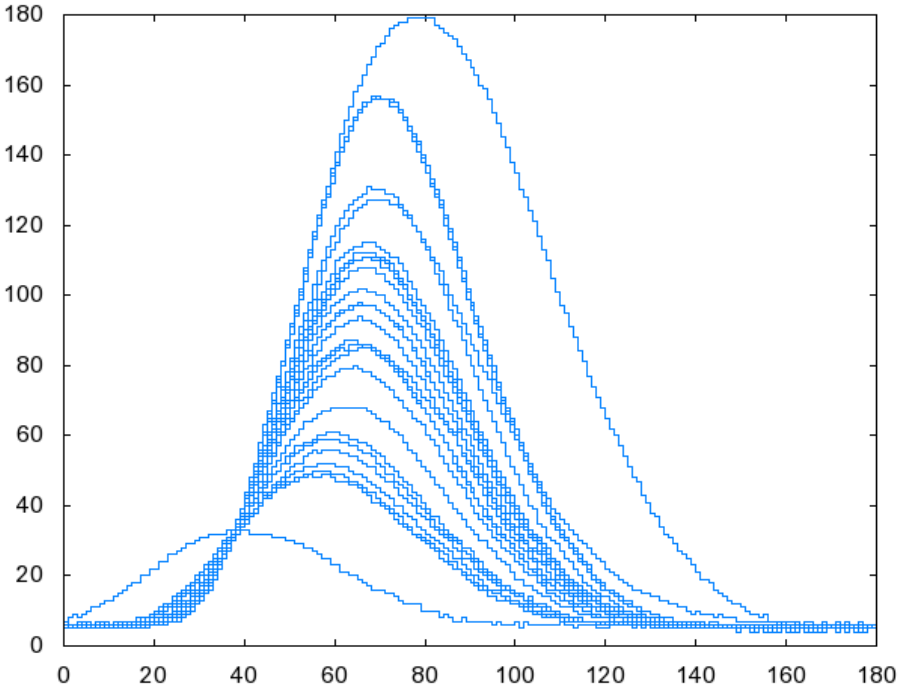
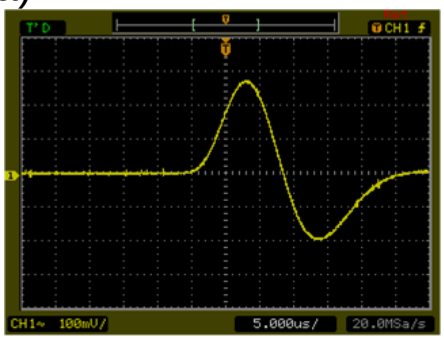


Figure 5: Many pulses has the same trigger point

3. Compare with oscilloscope:

The set up of this experiment is the same as that of device control experiment. In this work, we only compare the visual pulse shape that shown by oscilloscope and FADC kit. The comparison value by value would be a further development.

(a)



(b)

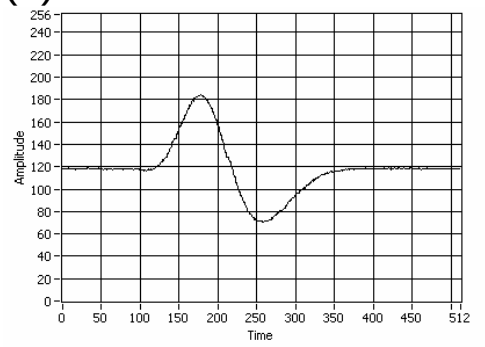
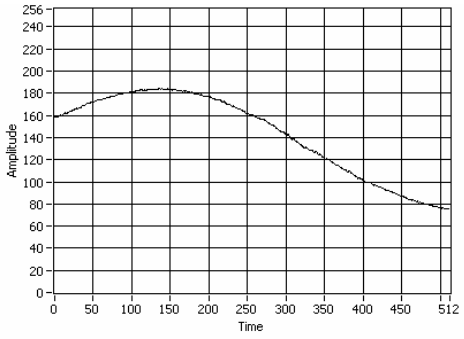


Figure 6: compare between oscilloscope(a) and FADC(b)

(a)



(b)

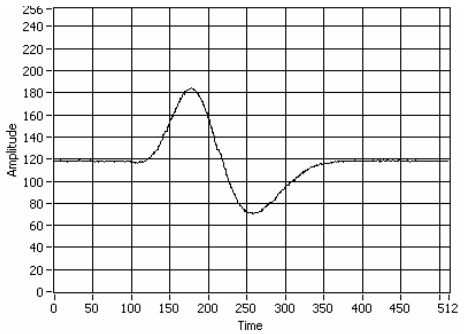


Figure 7: pulse shape obtained before(a) and after(b) change the time interval.

V. SUMARY:

Three main tests said above was a confirmation of the reliability of our device. The result of trigger experiment shows that many pulses had one same point which is the trigger point. Furthermore, not any pulse with amplitude lower than trigger was recorded. That means the trigger process works successfully. The result of device controlling experiment shows that this device can be configured to adapt many kinds of pulse shape. This make it is more flexible in using. In addition, in comparison with oscilloscope, the device showed its accuracy. Although it was only the visual comparison, in our recent tests, which compare value by value, the agreement between oscilloscope and our device is quite positive.

With high speed FADC, reconfigurable FPGA, the combination of them is an effort to apply the new electronic technology into nuclear research. The advantage of this combination is that the pulse shape can be known and analyzed. So, this device can directly connect to the output of detector without any other support devices as preamplifier, amplifier, discriminator, .etc. For further development, the USB can be a good replace for RS-232. Beside, the MCA can be developed using this device. Or the configuration of FPGA should be reviewed to make it better.

REFERENCES

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[2] http://www.altera.com
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[4] http://www.agilent.com
[5] http://www.canberra.com/products/