MULTICHANNEL ANALYZER (MCA) BASED ON FLASH-ADC AND FPGA FOR GAMMA RAY DETECTOR NaI(Tl)

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Abstract: In this article, we develop a gamma spectroscopy with the uses of a NaI(Tl) scintillation detector of 3inch x 3inch, and a multichannel analyzer (MCA) which is based on a Flash Analog-to-Digital Converter (Flash-ADC) 250 MHz-8bits and an embedded Field-Programmable Gate Array (FPGA) trigger. These hardware modules of Flash-ADC and embedded-FPGA trigger were designed and supported by Laboratory Masaharu Nomachi, Osaka University, Japan. The embedded VHDL (VHSIC Hardware Description Language) code for FPGA trigger, which was first developed by Nomachi's group, Osaka University, Japan for double beta measurement, is modified so that it works as a MCA with 4096 Digital Charge Integration (DCI) channels for gamma spectrometry NaI(Tl). A pulse generator and two standard radioisotope sources of ^{133}Ba and ^{152}Eu are used for evaluating the performance of the system. The development of the gamma spectroscopy NaI(Tl) will be used for gamma study in Department of Nuclear Physics, University of Science, VNU-HCMC.

Keywords: *Flash-ADC, FPGA, MCA, Gamma spectroscopy, VHDL*

1. INTRODUCTION

Radiation detection and measurement are principal techniques for nuclear and particle physics experiments. For many years, developing every part of a radiation spectroscopy has been the main considered feature which research groups, companies, universities, etc. have spent time in. In recent years, some experiments with spectroscopy using embedded-FPGA chip with Digital Pulse Processing (DPP) algorithm, and computer LabVIEW^{TM} interface aimed some advantages with better resolution in comparison with traditional analog chain, low-cost, and ease of migration of technology between different experiments [1],[2],[3],[4].

Since 2009, at Department of Nuclear Physics, Faculty of Physics and Engineering Physics, University of Science, HCMC, electronic readout system using free-running Flash-ADC and embedded-FPGA technology has been developed for nuclear radiation detector with 1-channel and multi-coincidence-channels input [4],[5].

In this work, we develop MCA (Flash-ADC/FPGA) for gamma spectroscopy NaI(Tl). The embedded VHDL code for FPGA module is built to perform some tasks such as triggering, Digital Pulse Processing, histogram memory, etc. A Computer interface based on LabVIEW^{TM} platform [6] is built for manipulation of triggering of parameters for pulse processing in FPGA, taking histogram data, plot histogram, etc. A pulse generator is employed to evaluate the dead-time of the system. Two standard radioisotopes ^{133}Ba and ^{152}Eu including multi gamma energies ranging from several tens KeV to MeV are used to figure the gamma response and energy resolution.

2. MULTI-CHANNEL ANALYZER MCA (FLASH-ADC 250MHz 8bits/FPGA)

The development of MCA (Flash-ADC/FPGA) is based on Flash-ADC 250MHz-8bit resolution and embedded FPGA. In this MCA, digital charge integration (DCI) channel describes the energy of gamma rays. An analog signal originated from a radiation detector is amplified by a pre-amplifier, shaping amplifier, and fed directly into Flash-ADC to convert a stream of digitized data. Digital pulse shape is recorded by FPGA trigger. DCI channel, which is calculated from digital pulse integration, is accumulated and stored in a histogram memory. The memory data is then transmitted to a computer via COM port RS-232.
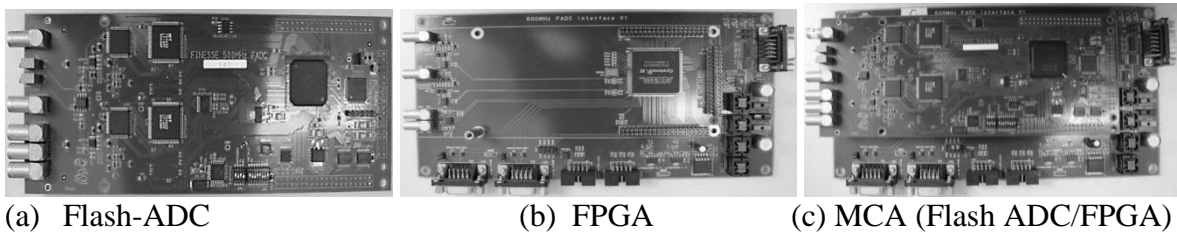
2.1 Flash-ADC and FPGA modules

(a) Flash-ADC (b) FPGA (c) MCA (Flash ADC/FPGA)

Fig.1. *Flash-ADC 250MHz 8-bits (a), FPGA (b) modules, and combination of two modules (c)*
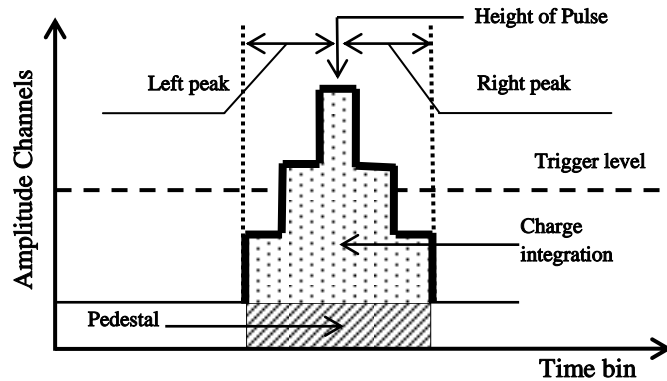

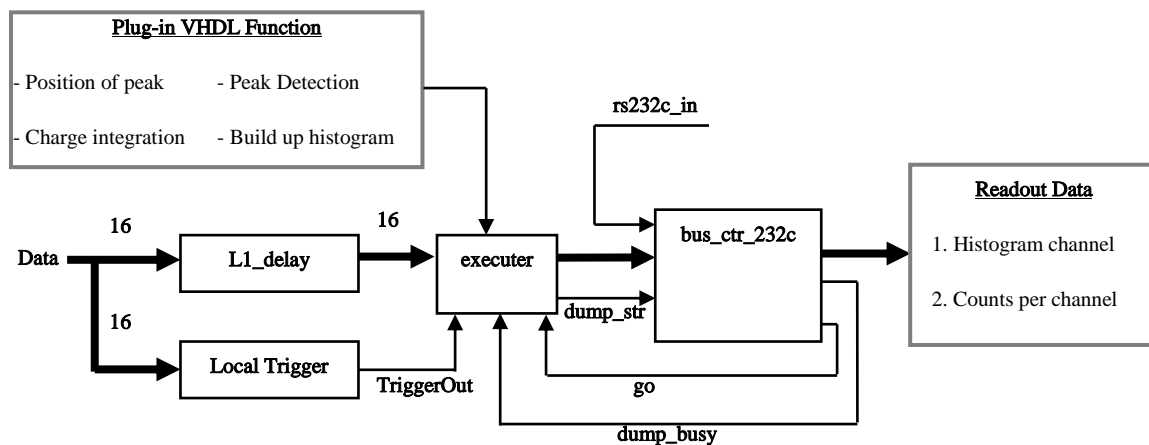**Fig 2**. *Parameter definition of a digital pulse*

Fig 3. *VHDL programming flow*

Flash-ADC 250MHz 8-bits has the voltage range 1000mV, 8 bits resolution (255 channels), and 250 MSamp/sec real-time sampling on two simultaneously sampled channels. Fig.1a is the circuit of Flash-ADC 250MHz 8-bits with two analog input channels. In this article, we use one channel for NaI(Tl) detector. Fig.1b is the embedded FPGA circuit with Cyclone II EP2C8Q208C7 FPGA chip, product of ALTERA, Co [7]. These hardware modules of Flash-ADC and FPGA were designed by Prof. Nomachi's group [3], are used for the development. Fig.1.c is the combination of modules of Flash-ADC and FPGA, and operated as a MCA.

2.2 The embedded VHDL code

Definition of parameters of a digital pulse is shown in Fig.2. Gamma energy deposited in the detector can be described through pulse height or charge integration. In this work, charge integration is used to describe for gamma energy. Because digital charge integration has better energy resolution compared to pulse height [4]. We build the embedded VHDL code for FPGA module, which can perform tasks of triggering, digital pulse processing for pulse integration, histogram memory, etc. With this development, the MCA can work with a histogram memory up to 4096 DCI channels. It is good enough for a scintillator detector NaI(Tl). Fig.3 shows the schematic diagram of FPGA plug-in programming. It consists of four components: L1_delay, Local_trigger, executer, and bus_ctr_232c.

2.3 LabVIEW™ interface

A computer interface for trigger controlling and data taking is written on LabVIEW™ (Laboratory Virtual Instrumentation Engineering Workbench) platform version 8.5, a software product of National Instruments, Ins. [7]. The front panel of computer LabVIEW™ interface is shown in Fig.4. The left hand side is for triggering and DPP controlling. The right hand side is displayer of histogram and data output. Recorded data is saved in a text file which can be used for post-analysis. The interface can be also acted as a digital oscilloscope for monitoring the pulse shape.
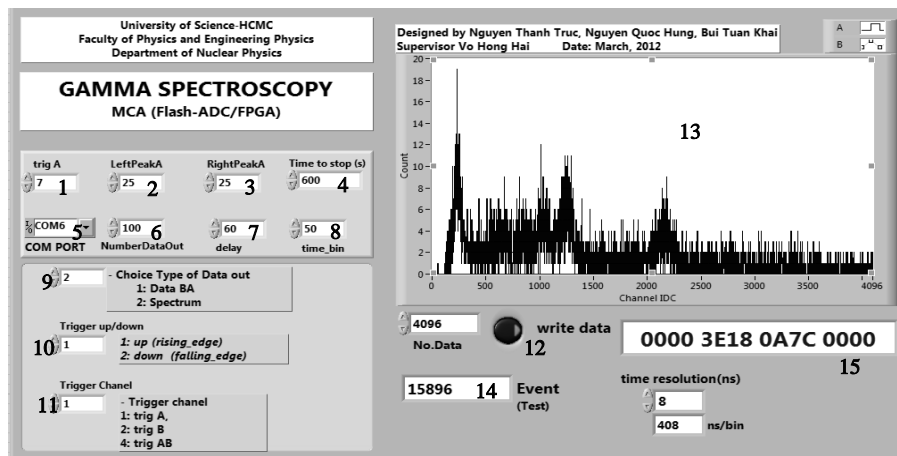

Fig.4. *LabVIEW™ interface with functions as an oscilloscope or a MCA*

(1)   TrigA: sets trigger for input data.
(2)   LeftPeakA: number of samples on the left side of the peak.
(3)   RightPeakA: number of samples on the right side of the peak.
(4)   Time to stop (s): time for one experiment.

(5)   COM PORT: select the computer's COM PORT where data is transmitted to.
(6)   Number Data Out: the size of the buffer used to store digitized data of a pulse.
(7)   Delay: the number of buffer's elements between written datum and read datum.
(8)   Time_bin: the interval between two times of detecting events.
(9)   Type Data out: mode to display output data.
(10)   Trigger up/down: mode to trigger rising edge or falling edge.
(11)   Trigger Channel: choose input channel(s): single channel or two simultaneous channels from Flash-ADC
(12)   Write data: if this button is pressed, the computer interface program writes data into a file.
(13)   Presenter: presents pulse signals or spectrum.
(14)   Counts of events: presents the number detected events in an acceptable range.
(15)   Transmitted data: presents number of events, channel, and counts per channel.

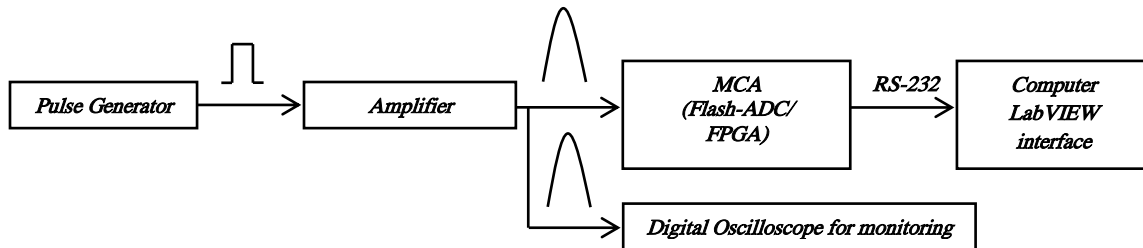## 3. EVALUATE TIME RESPONSE OF THE SYSTEM WITH PULSE GENERATOR

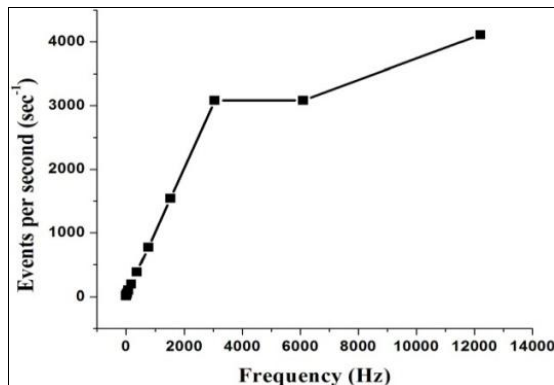**Fig.5**. *Time response evaluation with pulse generator*

Fig.6. *Time response of the system*

Table 1. *Time response of the system*

Frequency (Hz)	Recorded events/sec (sec^{-1})
12	12.05
95	96.33
381	385.29
1526	1541.12
3052	3082.24
6104	3082.24
12207	4109.96

A pulse generator, which generates a square pulse sharp with 80 nsec-width and frequency changeable, is fed into a shaping amplifier, type CANBERRA 2026 amplifier [8], and then connected to the input channel of MCA (Flash-ADC/FPGA). Data out from FPGA module is connected to computer via COM port RS-232 for data recording. Shaping-time parameter of the amplifier is set at 6μsec, which is also used for gamma measurements later. A digital oscilloscope is used for pulse monitoring. Fig.5 shows the schematic arrangement of time response measurement for the system. To evaluate the time response of the system, we use the pulse generator with pulse's frequency varying from Hz to MHz. Obtained results of time response are shown in Table 1 and plotted Fig.6. We can see that there is no dead-time of the system up to 3.050 Hz. In comparison to commercial MCA products of Canberra or Ortec, time response of this system is not so high. The reason of slow time response is due to slow data flow

of COM port RS-232 connecting between the FPGA module to computer. The data flow of inside FPGA chip itself is much higher with 50.000 Hz. However, for our purpose for gamma spectroscopy with low dose rate, the system is good enough.

4. GAMMA MEASUREMENT WITH SCINTILLATOR DETECTOR NaI(Tl) 3in. x 3in.

Fig.7 shows schematic arrangement for gamma measurements using the scintillator NaI(Tl) 3inch x 3inch. The scintillator detector is supplied with a positive high voltage of 0.8 kV from CANBERRA 3106D high voltage supply [8]. Analog signal from detector is amplified and time-shaped with $6\text{-}\mu\text{sec}$ by the shaping time amplifier, type CANBERRA 2026 amplifier, and then connected to MCA (Flash-ADC/FGPA). Two standard radioisotopes of ^{133}Ba $(0.1\mu\text{Ci})$ and ^{152}Eu $(1.05\mu\text{Ci})$, manufactured by Spectrum Techniques, Ins. [9], are used to do gamma measurements.
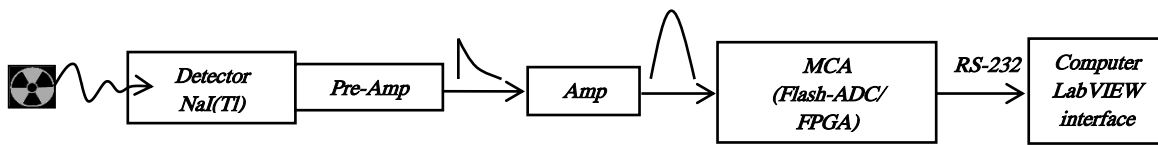

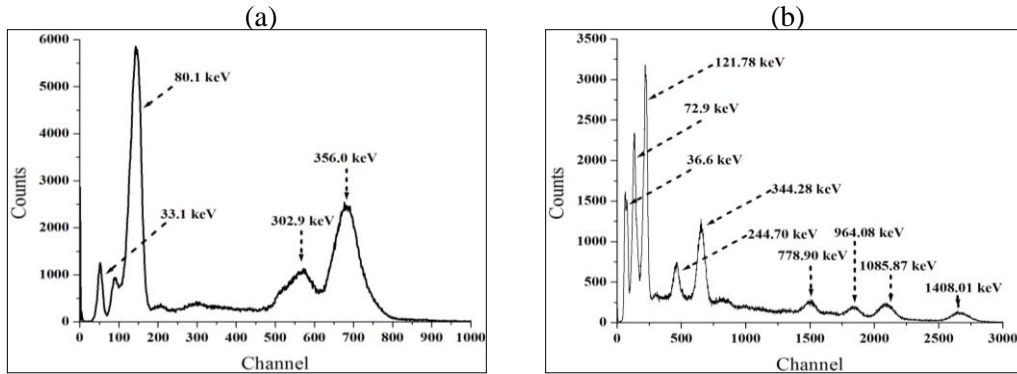**Fig.7**. *Schematic diagram of gamma spectroscopy using NaI(Tl) detector*

(a) (b)

Fig.8. *Gamma spectra from radioisotopes ^{133}Ba (a) and ^{152}Eu (b)*
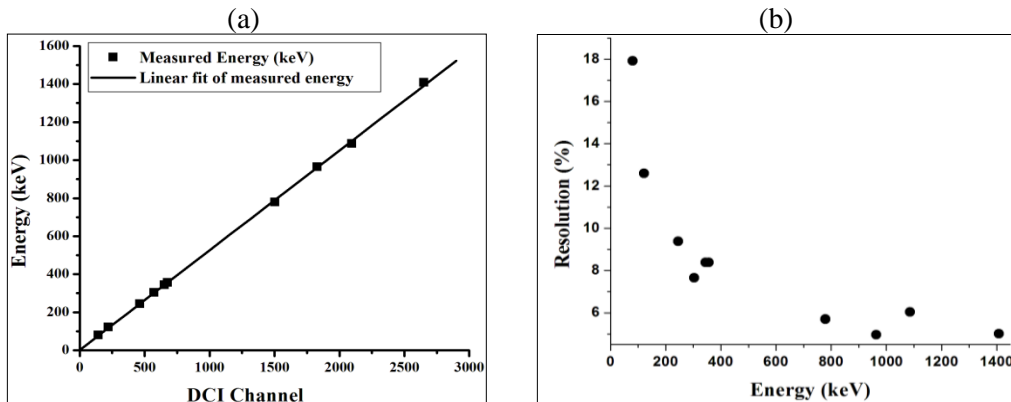
(a) (b)

Fig.9. *Energy calibration (a). Energy resolution as a function of gamma energy (b)*

Table 2. *Obtained results for photo-peak energies of* ^{133}*Ba and* ^{152}*Eu sources*

Radioisotopes	Energy (keV)	Channel	FWHM	R (%)
^{152}Eu	121.78	220	27.9	12.6
	244.7	462	43.3	9.4
	344.28	653	54.8	8.4
	778.9	1503	85.3	5.7
	964.08	1830	91.0	4.9
	1085.9	2096	126.1	6.0
	1408	2650	133.3	5.0
^{133}Ba	80.1	143	25.6	17.9
	302.9	572	43.2	7.6
	356	677	57.1	8.4

From gamma spectra of ^{133}Ba and ^{152}Eu, shown in Fig.8a and Fig.8b respectively, we can evaluate the peak positions (mean), and Full Width Half Maximum (FWHM) for several photo-peak energies rangeing from tens keV to MeV. Table 2 shows obtained data of peak position and FWHM. Fig.9a and Fig.9b show the energy calibration, and energy resolution of the system. The gamma spectroscopy NaI(Tl) shows good linerity response.

5. CONCLUSION

In this work, we develop the MCA read-out system using the Flash-ADC 250MHz/8-bits and embedded FPGA technology for gamma spectroscopy NaI(Tl). The hardware Flash-ADC and FPGA boards, which were designed by Prof. Nomachi's group, Osaka University, Japan, are used for the development. The embedded VHDL code with digital pulse processing is developed to perform a multi channel analyzer MCA with 4096 DCI channels. The computer LabVIEW interface is programmed to interact with the FPGA chip for trigger controlling and data taking. A pulse generator with pulse's frequency from Hz up to 12 MHz is used to evaluate the time response or dead-time of the system. The result shows that the system has no dead-time up to 3.050 Hz. It is not so high compared to commercial MCA products of Canberra and Ortec. The slow time response of the system is known as the limitation of COM port RS-232. However, for our purpose of gamma study with low dose rate, the system is good enough. Gamma measurements using NaI(Tl) 3inch x 3inch detector is carried out with two standard isotopes ^{133}Ba and ^{152}Eu. From obtained spectra, we evaluate the gamma response of the system such as the lineartiy and energy resolution.

ACKNOWLEDGES

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